In the Claims:

1. (Currently amended) A method of planarizing active layers of devices on a semiconductor structure comprising the steps of:

providing a semiconductor structure, said semiconductor structure having a top layer of dielectric material and areas of metallization defined in the top surface of said top layer of dielectric material;

depositing tunneling magneto-resistance "TMR" [[TMR]] devices at selected locations over said areas of metallization, said TMR devices having a known height above said top surface of said top layer of dielectric material;

depositing a first dielectric layer over said top surface of said top layer of dielectric [[layer]] material and over said ~~semiconductor~~ TMR devices;

forming a dummy layer of dielectric material over said first dielectric layer to a thickness equal to said known height of said ~~active semiconductor~~ TMR devices;

forming a dummy structure pattern mask over said dummy layer of dielectric material;

etching said dummy layer of dielectric material selective to said first dielectric layer so as to leave portions of said dummy layer as dummy structures on said top surface of said top layer of [[said]] dielectric material, said dummy ~~structure~~ structures having a height equivalent to said known height; and

depositing another layer of dielectric material over said ~~active semiconductor~~ TMR devices and said dummy structures, said another layer of dielectric material having a thickness at least greater than said known height of said ~~semiconductor~~ TMR devices.

2. (Currently amended) The method of claim 1 wherein the semiconductor structure is according to an XPC (cross point memory cell) architecture, and the TMR ~~elements~~ devices are deposited directly on top of the metallization.

3. (Currently amended) The method of claim 1 wherein the semiconductor structure is according to an FET architecture, the metallization is covered by a thin insulation layer, the TMR ~~elements~~ devices are deposited on top of said thin insulation layer and are connected by a local interconnect to an adjacent read wire.

4. (Currently amended) The method of claim 1 wherein said TMR ~~structure~~ devices ~~comprises~~ comprise at least two layers of metallization.

5. (Currently amended) The method of claim 1 wherein said first dielectric ~~conformal~~ layer is resistant to the diffusion of copper atoms and ions.

6. (Currently amended) The method of claim [[3]] 1 wherein said step of depositing a first dielectric layer comprises the step of depositing a layer selected from the group consisting of silicon nitride (Si_3N_4), ~~Silicon~~ silicon oxy nitride (SiON), silicon carbide (SiC) and aluminum oxide (Al_2O_3).

7. (Currently amended) The method of claim [[3]] 1 wherein said step of depositing another layer of dielectric material comprises the step of depositing a layer of silicon oxide (SiO_2).

8. (Currently amended) The method of claim [[3]] 1 wherein said step of depositing another layer of dielectric material comprises the step of depositing a layer of a low K dielectric.

9. (Currently amended) The method of claim [[5]] 7 further comprising the steps of:

etching wire trenches in said silicon oxide layer down to said ~~coating of silicon nitride;~~ first dielectric layer;

further etching vias through said ~~coating of silicon nitride~~ first dielectric layer in selective ones of said trenches to said [[lines]] areas of metallization in said top layer of dielectric material; and

filling said trenches and vias with a conductive metal.

10. (Currently amended) The method of claim [[7]] 9 wherein said steps of etching trenches and vias ~~comprises~~ comprise forming an etch mask with lithography and reactive ion etching said silicon oxide layer.

11. (Currently amended) The method of claim 1 wherein said step of etching said ~~another~~ dummy layer of dielectric material comprises the step of patterning a hardmask with MUV (mid-ultraviolet) lithography and etching said ~~another~~ dummy layer of dielectric material with an oxide etch selective to silicon nitride.

12. (Currently amended) The method of claim 1 wherein said active ~~semiconductor~~ layers of devices include Tunnel Junction devices.

13. (Currently amended) The method of claim [[8]] 9 wherein said conductive metal is copper.

14. (Currently amended) The method of claim 1 wherein said step of etching said dummy ~~structures~~ layer of dielectric material comprises the steps of depositing said dummy layer of dielectric material to a thickness equivalent to said known height, and etching to remove all of

said dummy layer of dielectric material except those portions protected by [[the]] a photoresist mask.

15. (Currently amended) The method of claim 1 wherein said step of depositing ~~active semiconductor elements~~ TMR devices is according to [[the]] pattern factor rules for fill structures ~~and during planarization for MRAM structures~~ and said step of ~~forming dummy structures~~ etching said dummy layer of dielectric material follows less stringent rules and uses MUV (Mid-UltraViolet) lithography.

16. (Currently amended) The method of claim [[7]] 9 further comprising the step of depositing a coating of TaN (tantalum nitride) over said trenches and said vias.

17. (Currently amended) The method of claim [[4]] 1 wherein said step of etching said dummy [[structures]] layer of dielectric material comprises the [[step]] steps of ~~depositing~~ forming said dummy layer of dielectric material to a thickness substantially equal to said known height, etching said dummy layer with a process selective to said first ~~conformal~~ dielectric layer and stripping [[said]] a photoresist mask to leave said dummy structures.